RN8209G User Manual

Data: 2009-5-13

Rev: 1.0

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1 Introduction

1.1 Features

√ Measurement

- Three channels of Σ-△ ADC are provided.
- The active energy accuracy is less than 0.1% (< 0.1%) over a dynamic range of 1500:1 with the IEC62053-22: 2003 Standard supported.
- The reactive energy accuracy is less than 0.1% (< 0.1%) over a dynamic range of 1500:1 with the IEC62053-23: 2003 Standard supported.
- Two-channel current and one-channel voltage RMS is provided, with the RMS accuracy <0.5% over the 400:1 dynamic range.
- No-load threshold is adjustable.
- Reverse active power indication is provided.
- Provide voltage channel frequency measurement.
- Provide voltage channel zero-crossing detection.

√ Software meter calibration

- The meter constant (HFConst) is adjustable.
- Gain and phase calibration is provided.
- Offset calibration is provided for active, reactive and RMS.
- Reactive phase calibration is provided.
- Acceleration is provided for small-signal meter calibration.
- Automatic checksum is provided for configuration parameters.

√ SPI / RSIO interfaces are provided

√ Power supply monitoring is provided

√ Single +5 V power supply with the typical power consumption value of 32mW

√ Built-in 2.5V ± 3% reference voltage, with typical temperature coefficient of 25ppm / ℃

√ SSOP24 lead-free package is adopted.

1.2 Functions

RN8209G can measure active power, reactive power, active energy and reactive energy, and can provide two-channel independent active power and RMS, voltage RMS, line frequency, zero-crossing interrupt, etc. to achieve flexible anti-tampering solutions.

RN8209G supports all-digital gain, phase and offset calibration, with the active and reactive energy pulses respectively output from the pins of PF and QF.

RN8209G provides two serial interfaces SPI and RSIO, to facilitate communication with the external MCU, in which RSIO is RENERGY's proprietary single-wire communication interface, able to achieve two-channel communication based on a single data cable.

The internal power supply monitoring circuit of RN8209G can ensure reliable operation of the chip when power on and off.

1.3 Block Diagram of Functions

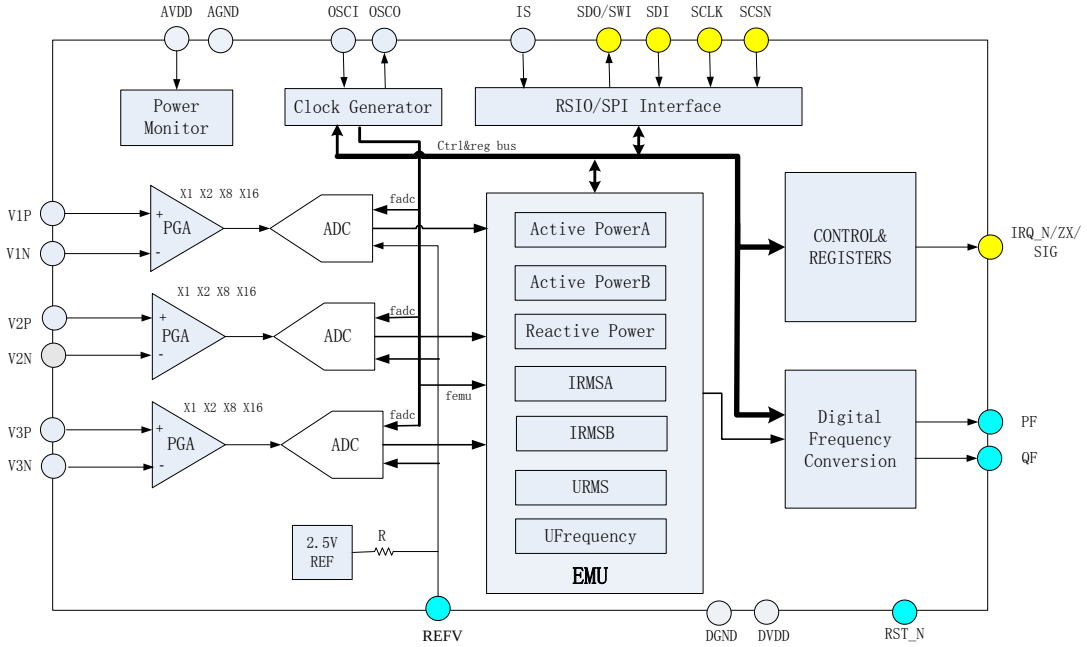


Figure 1-2 Block Diagram of system

1.4 Pin Definitions

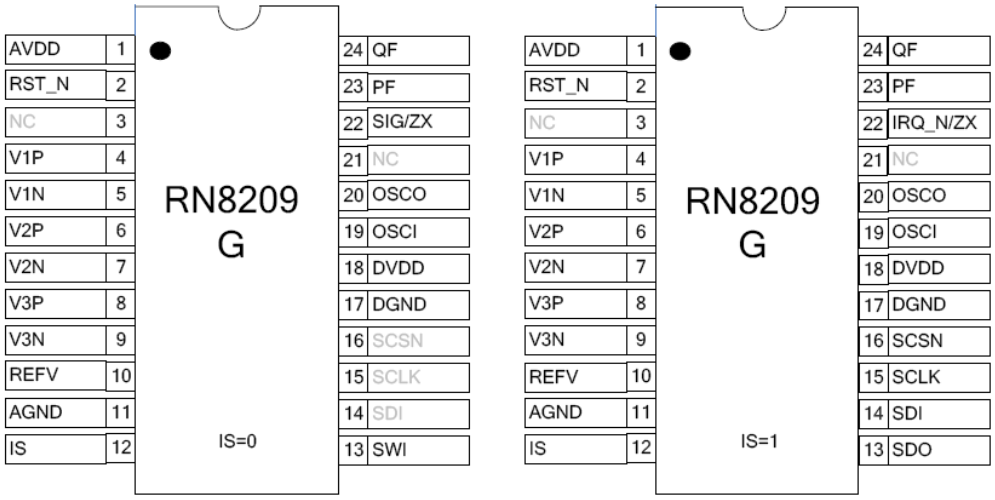


Figure 1-2 Pin Assignment

Table 1-1 RN8209G Pin Functions

Pins	Signs	Features	Function Descriptions
1	AVDD	Power supply	The pin of analog power supply is used to provide power supply to the analog portion of the chip. This pin should use an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 4.5V-5.5V.
2	RST_N	Input	Reset pin, active at a low level. When at a low level, the chip is in a reset state. The pin should be connected to an external pull-up resistor.
3	NC	NC	Not connected
4,5	V1P, V1N	Input	Positive and negative analog input pins of current Channel A - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 700mV, and the maximum withstand voltage is ± 6V.
6,7	V2P, V2N	Input	Positive and negative analog input pins of current Channel B - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 700mV, and the maximum withstand voltage is ± 6V.
8,9	V3P,V3N	Input	Positive and negative analog input pins of the voltage channel - A fully differential input mode is adopted, the maximum input in normal operation Vpp is ± 700mV, and the maximum withstand voltage is ± 6V.
10	REFV	Input/Output	2.5V reference voltage input and output pins – The external reference source can be directly connected to this pin. Whether internal or external reference source is adopted, this pin should use a 10μF capacitor and a 0.1μF capacitor paralleled for decoupling.
11	AGND	Power supply	Analog ground
12	IS	Input	Serial communication type selection pin – it is used to determine the communication interface type of the chip. If IS = 0, choose RSIO as the communication interface; if IS = 1, select SPI as the communication interface. Internal floating with external pull-up or pull-down
13	SDO/SWI	Input/Output	SDO and SWI multiplexed pins, 3.3V/5V compatible pins. SWI is the signal name of the RSIO bus. When IS = 1, this pin will be SPI serial data output SDO. After reset, this pin features a high impedance output. When IS = 0, this pin is the input/output pin SWI of the single-line communication. After reset, this pin is for input and when the MCU command is responsed by the SWI pin, this pin will change to be an output for data transmission. With a built-in pull-up resistor.
14	SDI	Input	When IS = 1, this pin will be an SPI serial data input pin, as well as a 3.3V/5V compatible pin. When IS = 0, this pin has a pull-up resistor embedded.
15	SCLK	Input	When IS = 1, this pin will be an SPI serial clock input pin, as well as a 3.3V/5V compatible pin. When IS = 0, this pin has a pull-up resistor embedded.

16	SCSN	Input	When IS = 1, this pin will be for an SPI chip-select signal pin (active at a low level), as well as a 3.3V/5V compatible pin. Internal floating with external pull-up When IS = 0, this pin has a pull-up resistor embedded.
17	DGND	Power supply	Digital ground
18	DVDD	Power supply	Digital power supply pin - Used to provide power supply to the digital part. This pin should have an external 10μF capacitor and a 0.1μF capacitor paralleled for decoupling. The normal application range should be: 4.5V-5.5V.
19	OSCI	Input	Input terminal of external crystal or external clock input – The crystal frequency is typically 3.579545MHz.
20	OSCO	Output	Output terminal of external crystal - The OSCO pin can drive one CMOS load when OSCI has an external clock connected.
21	NC	NC	Not connected
22	IRQ_N /ZX/SIG	Output	Interrupt / zero-crossing detection / reset sign output pin - After reset, it will serve as an interrupt pin. When Zxcfg = 0 (EMUCON-bit7) with the SPI selected, it will serve as an interrupt request IRQ_N. When Zxcfg = 0 (EMUCON-bit7) with the RSIO selected, it will serve as an SIG signal. When Zxcfg = 1 (EMUCON-bit7), it will serve as ZX: voltage channel zero-crossing output.
23	PF	Output	Pulse output of active energy, low-level output by default. It's frequency will indicate the size of transient active power, able to achieve a 5mA output and current sinking.
24	QF	Output	Pulse output of reactive energy, low-level output by default. It frequency will indicate the size of transient reactive power, able to achieve a 5mA output and current sinking.

1.5 Typical Application

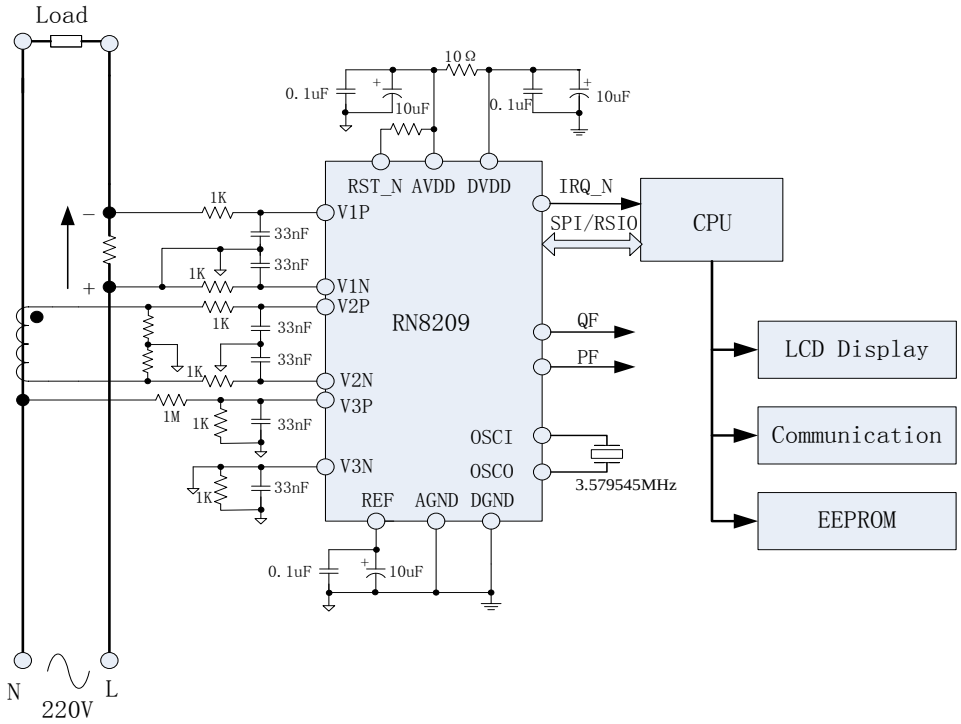


Figure 1-3 Typical Application of Single-phase Anti-tampering Meter

2 System Functions

2.1 Power Supply Monitoring

The RN8209G includes an internal power supply monitoring circuit, able to continuously monitor the analog supply (AVDD). When the power supply is lower than 4V ± 0.1V, the chip will be reset, and when the supply is higher than 4.3V ± 0.1V, the chip will work normally.

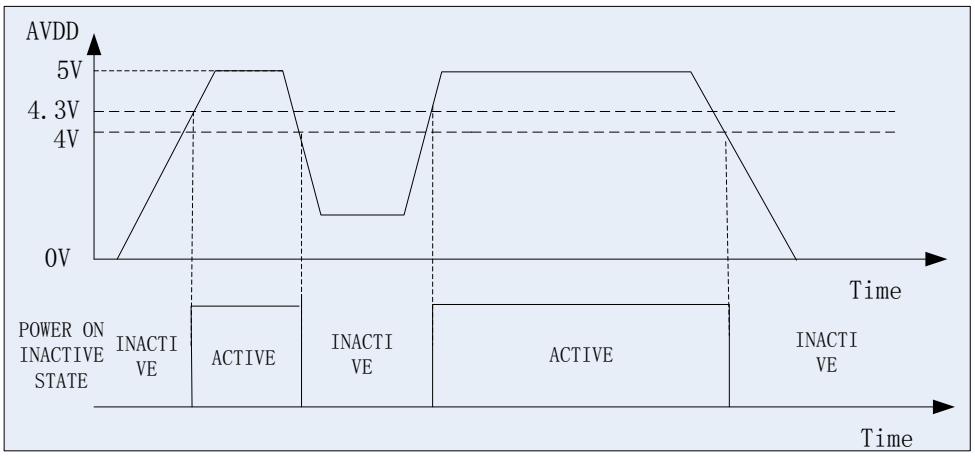


Figure 2-1 Power Detection Features

To ensure normal work of the chip, the AVDD fluctuations should not exceed 5V ± 5%.

2.2 System Reset

RN8209G supports two global reset methods:

- Power ON/OFF
- External pin reset

When any global reset occurs, the register will be restored to its reset initial value, and the external pins will have the level back to the initial state.

Relevant register:

In the system status register, RST is a reset sign: when the external RST_N pin or the power-on reset has ended, this bit will be set as 1, cleared after read and can be used as a meter calibration data request after reset.

2.3 Analog-digital conversion

RN8209G includes three channels of ADC, respectively used for phase current sampling, neutral current sampling and voltage sampling. The bit of ADC2ON in the system control register is used to open / close the current Channel B.

ADC uses a fully differential input. The current and voltage channels have the maximum signal input amplitude at 700mv of the peak.

By configuring bit5 ~ bit0 in the system control register (SYSCON 0x00H), the three channels of ADC can have the gain magnification configured separately as 1, 2, 8 or 16. The current Channel A has its gain magnification as 16 times by default.

2.4 Active Power

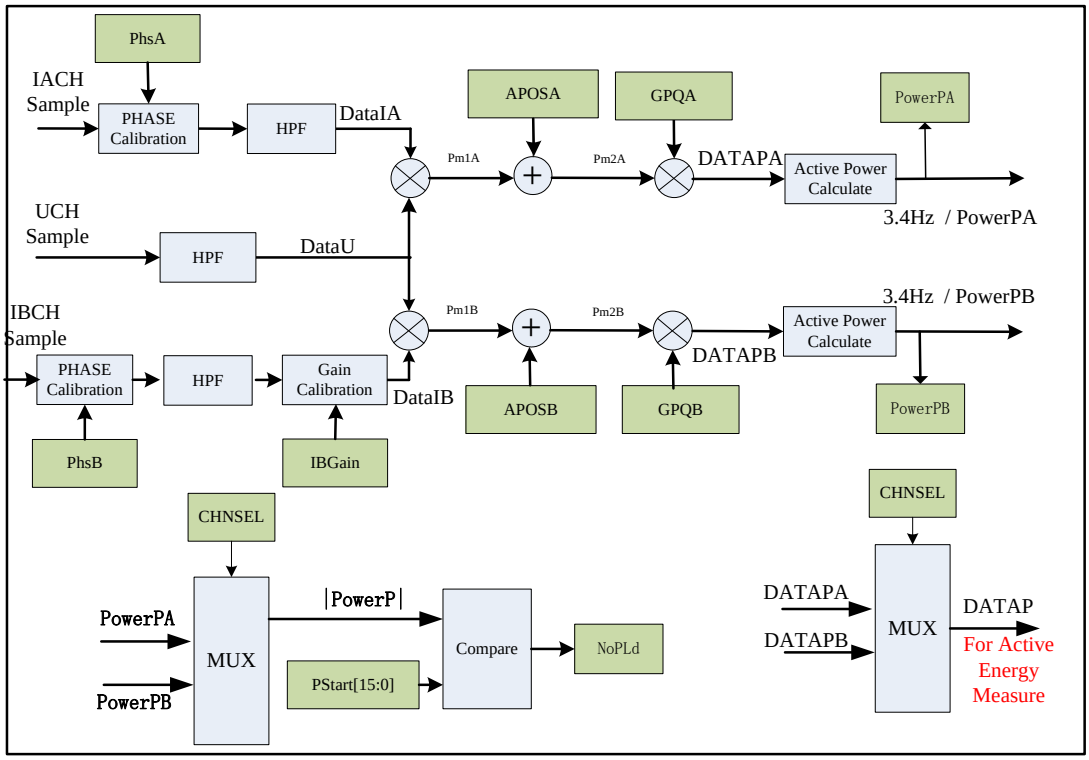


Figure 2-2 Active Power Diagram

RN8209G provides two channels of active power calculation and correction, respectively, the active power calculation and calibration of Current A and voltage, and the active power calculation and calibration of Current B and voltage.

Registers also contain two sets (A / B) of phase calibration, active offset calibration, active gain calibration and average power registers. In addition, in order to ensure the consistency of the two channels, it also provides the gain calibration register IBGain of the current channel B.

The special commands can be used to determine which channels of the average active power (PowerP) currently used to determine the no-load and start status, as well as the instantaneous active power channel (DATAP) currently used to calculate the active energy come from, with the details referring to the section related to special commands.

Users can select and configure the channels by means of special commands, and the configuration results can be queried by the CHNSEL register bit.

The digital high-pass filter in the diagram is mainly used to remove the DC component in current and voltage sampling data.

2.5 Reactive Power

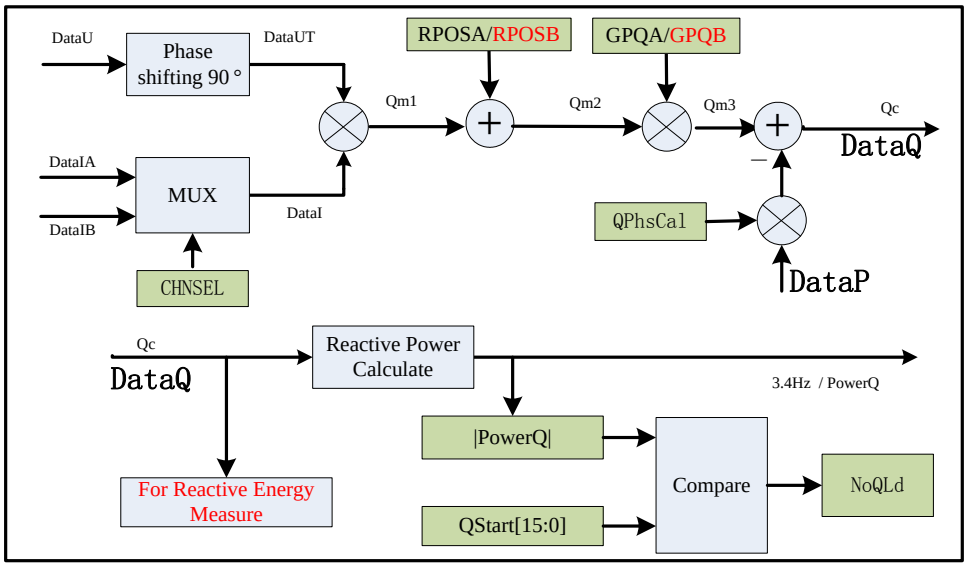


Figure 2-3 Reactive Power Diagram

RN8209G contains a circuit for reactive power measurement. Therein, the DataUT for measurement results from 90 degrees' phase shift of DataU; DataI comes from DataIA or DataIB, which can be configured by means of special commands, and the configuration results can be queried by the CHNSEL register bit.

2.6 RMS

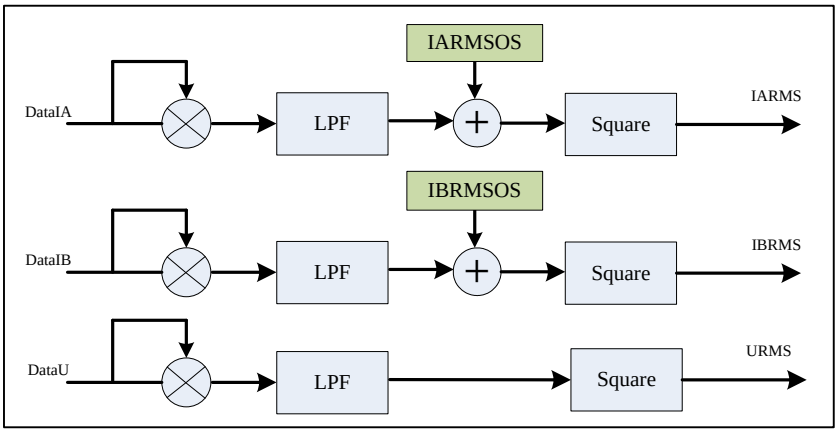


Figure 2-4 RMS Calculation Diagram

RN8209G provides the true RMS parameter output of three channels, including URMS, IARMS and IBRMS. The register length is 24bit, refresh once every 3.4HZ. In addition, it also includes two RMS Offset registers: IARMSOS and IBRMSOS.

Note: Channel 2 gain calibration (IBGain) will affect the IBRMS output, but phase calibration, power gain calibration and power offset calibration will have no effect of the RMS calculation results.

2.7 Energy Calculation

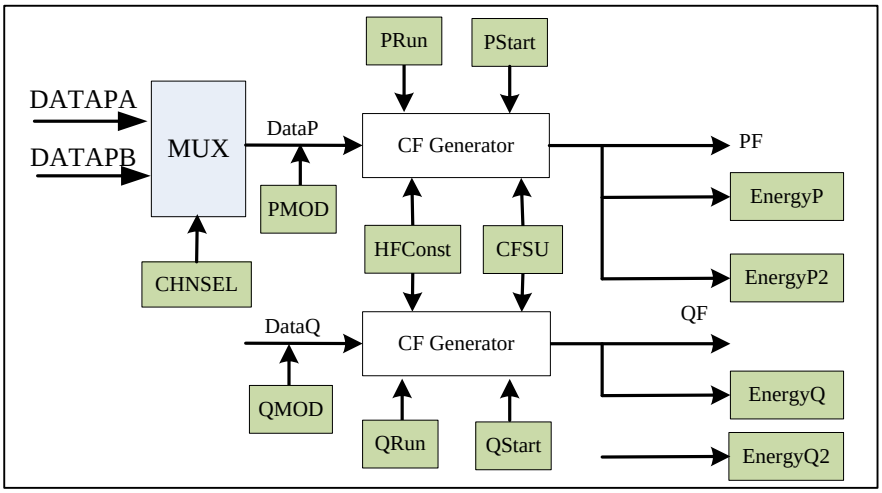
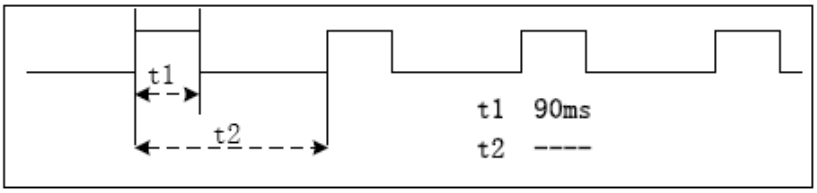


Figure 2-4 Energy Calculation

Energy pulse output:

The pulse output, namely, the meter calibration pulse output, can be directly connected to a standard meter for error comparison.

The PF / QF output meets the following timing relationship:



Note: When the pulse output period is less than 180ms, the pulse will be output in form of equal duty.

PFcnt, HFConst, pulse output and energy registers have the relationship as follows:

When 2*|PFcnt| (0x20H) = HFConst (0x03H), PF has a pulse output. Simultaneously, the energy registers EnergyP (0x29H) and EnergyP2 (0x2AH) will have 1 added respectively.

When 2*|QFcnt| (0x21H) = HFConst (0x03H), QF has a pulse output. Simultaneously, the energy registers EnergyQ (0x2BH) and EnergyQ2 (0x2CH) will have 1 added respectively.

Relationship among pulse output, energy register, PRun / QRun and PStart / QStart:

Active / reactive energy registers and PF / QF output are also controlled by PRun / QRun and PStart / QStart.

- When PRun = 0 or |P| is less than PStart, PF does not output any pulse; PFcnt and active registers will not be increased.
- When QRun = 0 or |Q| is less than QStart, QF does not output any pulse; QFcnt and reactive energy registers will not be increased.

Pulse output speedup:

To speed up the small-signal calibration, it provides the function of pulse output speedup. While correcting small signals, you can configure CFSUEN and CFSU [1:0] bits of the EMUCON (0x01H) register, so that the PF / QF output frequency could be increased, by 16 times at most.

Reverse direction:

When the active or reactive power is negative, the EMUStatus register will have its REVP bit or REVQ bit changed into 1, with REVP bit and PF pulse, as well as REVQ bit and QF pulse synchronously refreshed.

2.8 Channel Switch

RN8209G specially provides one channel of ADC used for measurement of neutral current RMS and active power, and provides the function to switch the phase current and neutral current channels for users to choose which current they like to measure the active energy / reactive energy / reactive power.

The current channels can be switched by means of special commands, with the details referring to the section for special command registers. The configuration results can be queried by the register bit CHNSEL.

2.9 Frequency Measurement

RN8209G can directly output line frequency parameter (UFreq 0x25H), measurement of fundamental frequency and measurement bandwidth of 250Hz.

2.10 Zero-crossing Detection

Configure ZXCFG (EMUCON.7) and select pins IRQ_N / ZX / SIG to enable / disable zero-crossing output.

Configure ZXD1 (EMUCON.9) and ZXD0 (EMUCON.8) register bits to select four kinds of zero-crossing output.

2.11 Interrupt

When the communication interface has selected **SPI**, the **RN8209G** interrupt resources include **1** interrupt-enabled register IE, **2** interrupt status register **IF** and **RIF**, and 1 multiplexed interrupt request pin **IRQ_N / ZX / SIG.**

When the communication interface has selected **RSIO**, the **IRQ_N / ZX / SIG** pin will have its interrupt function closed up; **IE** and **RIF** registers will also be closed up, but the **IF** register will be reserved and defined as an event identification register.

1. Process **for SPI** to read **RIF** register

The timing for MCU to read RIF operations is shown in Figure 2-5:

1) Driven by the SCLK clock, MCU will give command to read the registers via the SDI pin, it will clear interrupt status register IF when meet the SCLK falling edge of the last bit (LSB) of read command byte, at this time, the RIF register will have its contents remaining unchanged and meanwhile IRQ_N will change from a low level to a high level.

2) The chip responds to read the RIF command and move the RIF register contents out of the SDO pin driven by the SCLK clock. In this process, the RIF always keeps the same as the value before reading operations, while the IF register can receive new interrupts in this process of the SPI.

3) After the last bit has been moved out of the SDO and when the SCSN is changing from low to high, the contents of the RIF register and IF will be synchronized.

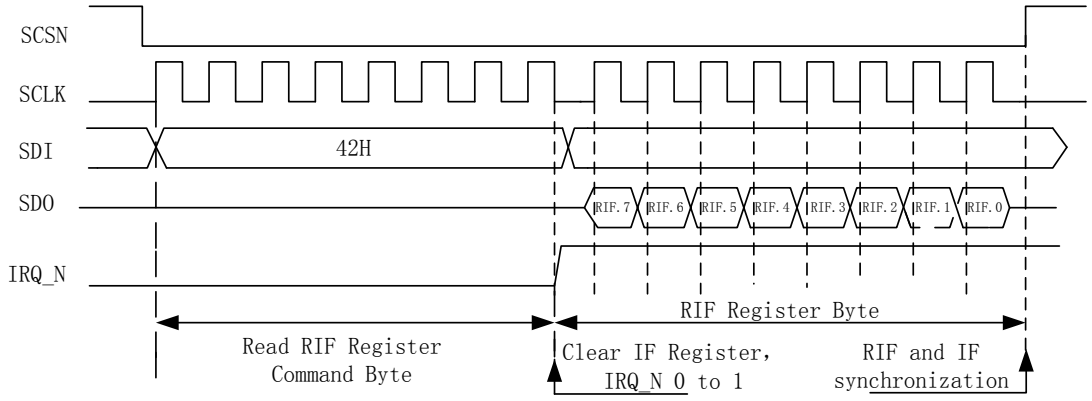


Figure 2-5 Timing Diagram for RIF Register Reading

In addition to RIF register reading operation, the IF and RIF will remain the same under other circumstances. To avoid losing interrupts while the SPI is reading interrupt flags, it is recommended that users use the RIF registers in the interrupt handler.

2. Interrupt request signal IRQ_N

When IS = 1, IRQ_N / ZX / SIG pin is multiplexed by IRQ_N and zero-crossing detection output ZX, and the use of this pin can be determined by configuring the ZXCFG bit of EMUCON register (0x01H).

When the interrupt has enabled the corresponding interrupt permit bit of the register with interrupt events occurring, the IRQ_N pin will be at a low level. When the CPU reads RIF via the SPI interface, it will first write the command register, the IRQ_N pin will back to a high level when meet the SCLK falling edge of the last bit (LSB) of the command byte, as shown in Figure 2-5.

When IS = 0, that is, when the communication interface is selected as the RSIO, the IRQ_N / ZX / SIG pin will be multiplexed by SIG and ZX, with the default state of the signal SIG.

3. Interrupt Processing

Hardware:

- The IRQ_N of RN8209G is usually connected to the MCU external interrupt pin /INT, and when IRQ_N is changing from high to low, the MCU will generate the /INT interrupt.
- The MCU serves as a SPI host, while RN8209G as an SPI slave.

Interrupt handler:

Step 1: MCU interrupt initialization

1. The MCU reads RN8209G RIF to clear IF and RIF interrupt flags;

2 Configure RN8209G IE register to enable the necessary interrupt permit bit to generate IRQ_N;

3. The MCU enables the / INT external interrupt to wait for RN8209G interrupt event occurring. The

IRQ_N output triggers the / INT interrupt, and jump into the /INT interrupt entry address.

Step 2: MCU interrupt service procedure

1 Close MCU global interrupt and /INT interrupt;

2. The MCU reads RIF register via the SPI to clear the IF and RIF registers and have the IRQ_N back to a high level.

3. The MCU determines RN8209G interrupt source by determining the RIF interrupt flag, and then execute the corresponding interrupt handler. In this process, if RN8209G has any new interrupt event, the related flag bit in IF set 1， IRQ_N will also change from high to low, trigger the MCU / INT interrupt flag set 1 and record this event.

4. After the interrupt handler has been executed, the MCU will open the global interrupt and /INT interrupt, and have the interrupt back after the site has been restored.

After interrupt return, if any /INT interrupt flag is detected, the program will enter the external interrupt ISR, and repeat 2. If no /INT interrupt flag is detected, it indicates that there is no interrupt event occurring in interrupt processing, and the program will continue.

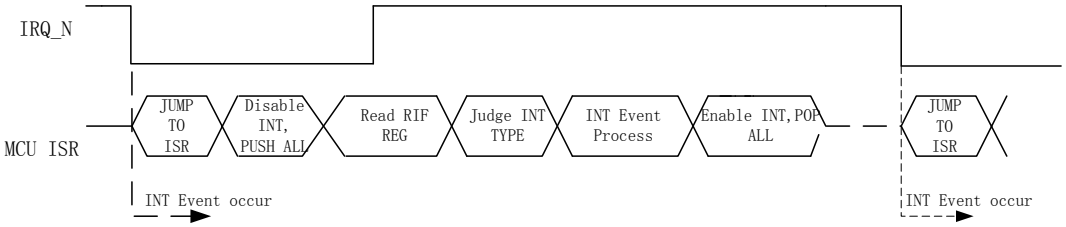


Figure 2-6 RN8209G Interrupt Processing

When the communication interface is selected as RSIO, the MCU can query the IF register via the RSIO interface to determine whether appropriate event has happened and then implement the appropriate event handler.

2.12 Register

2.12.1 List of Registers

Table 2-3 List of RN8209G Registers

Address	Name	R/W	Word Length	Reset Value	Descriptions
Calibration Parameter and Measurement Control Registers					
00H	SYSCON	R/W	2	0003h	System control register, write-protect
01H	EMUCON	R/W	2	0003h	Energy measure control register, write-protect
02H	HFConst	R/W	2	1000h	High frequency impulse const register, write-protect
03H	PStart	R/W	2	0060h	Active power start threshold setup register, write-protect
04H	QStart	R/W	2	0120h	Reactive power start threshold setup register, write-protect
05H	GPQA	R/W	2	0000h	Channel A power gain register, write-protect
06H	GPQB	R/W	2	0000h	Channel B power gain register, write-protect
07H	PhsA	R/W	1	00h	Channel A phase calibration register, write-protect

08H	PhsB	R/W	1	00h	Channel B phase calibration register, write-protect
09H	QPhsCal	R/W	2	0000h	Reactive power phase calibration, write-protect
0AH	APOSA	R/W	2	0000h	Channel A active power offset register, write-protect
0BH	APOSB	R/W	2	0000h	Channel B active power offset register, write-protect
0CH	RPOSA	R/W	2	0000h	Channel A reactive power offset register, write-protect
0DH	RPOSB	R/W	2	0000h	Channel B reactive power offset register, write-protect
0EH	IARMSOS	R/W	2	0000h	Current Channel A RMS offset calibration, write-protect
0FH	IBRMSOS	R/W	2	0000h	Current Channel B RMS offset calibration, write-protect
10H	IBGain	R/W	2	0000h	Current Channel B gain setting, write-protect
Measurement Parameter and Status Registers					
20H	PFCnt	R/W	2	0000h	Active energy counter register, write-protect
21H	QFCnt	R/W	2	0000h	Reactive energy counter register, write-protect
22H	IARMS	R	3	000000h	Current A RMS
23H	IBRMS	R	3	000000h	Current B t RMS
24H	URMS	R	3	000000h	Voltage RMS
25H	UFreq	R	2	0000h	Voltage frequency
26H	PowerPA	R	4	00000000h	Active Power A
27H	PowerPB	R	4	00000000h	Active Power B
28H	PowerQ	R	4	00000000h	Reactive power
29H	EnergyP	R	3	000000h	Active energy, not cleared after read
2AH	EnergyP2	R	3	000000h	Active energy, cleared after read
2BH	EnergyQ	R	3	000000h	Reactive energy, not cleared after read
2CH	EnergyQ2	R	3	000000h	Reactive energy, cleared after read
2DH	EMUStatus	R	3	00EE79h	Energy measurement status and checksum register
Interrupt Registers					
40H	IE	R/W	1	00h	Interrupt enable register, write-protect
41H	IF	R	1	00h	Interrupt flag register, cleared after read
42H	RIF	R	1	00h	Reset interrupt flag register, cleared after read
System Status Registers					

43H	SysStatus	R	1	--	System status register
44H	RData	R	4	--	Previous SPI / RSIO data read out
45H	WData	R	2	--	Previous SPI / RSIO data written
7FH	DeviceID	R	3	820900h	RN8209G Device ID

2.12.2 Calibration parameter registers

System control registers

SYSTEM Control Register (SYSCON) Address: 0x00 H Default Value: 0003H		
Bit	**Bit Name**	**Descriptions**
15-7	Reserved	Not writable, read as 0. The SYSCON register still operates according to 2 byte registers.
6	ADC2ON	ADC2ON = 1: it means that ADC has its current Channel B open; = 0: it means that ADC has its current Channel B closed, and ADC output is a constant of 0.
5-4	PGAIB[1:0]	Analog gain selection of current Channel B PGAIB1 / PGAIB0 / Current Channel B 0 / 0 / PGA=1 0 / 1 / PGA=2 1 / 0 / PGA=8 1 / 1 / PGA=16
3-2	PGAU[1:0]	Voltage channel analog gain selection, configuration options same as PGAIB.
1-0	PGAIA[1:0]	Current Channel A analog gain selection, configuration options same as PGAIB, 16 times by default.

Measurement Control Registers

Measurement control registers are used for settings of energy measurement functions.

Energy Measure Control Register (EMUCON) Address: 0x01 H Default Value: 0003H		
Bit	Bit Name	Descriptions
15-14	Reserved	Read as **0**
13-12	QMOD[1:0]	Reactive energy accumulation mode selection: QMOD1 / QMOD0 / Accumulative power Qm 0 / 0 / If Qm = DataQ, the positive and negative power will be involved in accumulation, and the negative power will have an REVQ symbol. 0 / 1 / Only positive power is accumulated. 1 / 0 / If Qm=|DataQ|, the positive and negative power will be involved in accumulation, and the negative power will have no REVQ symbol. 1 / 1 / Qm = DataQ (reserved)
11-10	PMOD[1:0]	Active energy accumulation mode selection: same as the reactive energy accumulation in the table above.
9	ZXD1	When the ZX output initial value is 0, different waveforms will be output according

		to ZXD1 and ZXD0 configuration: When ZXD1 = 0, it means that only at the selected zero-crossing, the ZX output changes; When ZXD1 = 1, it means that at the positive and negative zero-crossing points, the ZX outputs changes.
8	ZXD0	When ZXD0 = 0, it means that the positive zero-crossing point is selected as a zero-crossing detection signal; When ZXD0 = 1, it means that the negative zero-crossing point is selected as a zero-crossing detection signal;
7	ZXCFG	ZXCFG = 0: when the interface is SPI, the pin IRQ_N / ZX / SIG serves as IRQ_N. ZXCFG = 0: when the interface is RSIO, the pin IRQ_N / ZX / SIG serves as a SIG. ZXCFG = 1: the pin IRQ_N / ZX / SIG serves as ZX.
6	HPFIOFF	HPFIOFF = 0: Enable IA and IB channel digital high-pass filters HPFIOFF = 1: Disable IA and IB channel digital high-pass filters
5	HPFUOFF	HPFUOFF = 0: Enable U-channel digital high-pass filters HPFUOFF = 1: Disable U-channel digital high-pass filters
4	CFSUEN	CFSUEN is the control bit of the PF / QF pulse output acceleration module. When CFSUEN = 1, the pulse acceleration module will be enabled, and the pulse output rate will be increased by 2^ (CFSU [1:0] +1) times. When CFSUEN = 0, the pulse acceleration module will be disabled, and the pulse will have normal output.
3,2	CFSU[1:0]	This bit will work with the help of CFSUEN. See CFSUEN instructions.
1	QRUN	When QRUN = 1, enable the QF pulse output and reactive energy register accumulation; When QRUN = 0, disable the QF pulse output and reactive energy register accumulation, with the default of 1.
0	PRUN	When PRUN = 1, enable the PF pulse output and active energy register accumulation; When PRUN = 0, disable the PF pulse output and active energy register accumulation, with the default of 1.

Pulse frequency registers

High Frequency Impulse Const Register (HFConst)				Address: 0x 02H Default Value : 1000H				
	Bit15	14	13	12	11	10	9	Bit8
Read: Write:	HFC15	HFC14	HFC13	HFC12	HFC11	HFC10	HFC9	HFC8
Reset:	0	0	0	1	0	0	0	0
:	Bit7	6	5	4	3	2	1	Bit0
Read Write:	HFC7	HFC6	HFC5	HFC4	HFC3	HFC2	HFC1	HFC0
Reset:	0	0	0	0	0	0	0	0

HFConst is a 16-bit unsigned number, it should be compared with 2 times of the absolute value of the fast pulse counter register PFCNT / QFCNT register value. If the result is greater than or equal to the HFConst, then there will be corresponding PF / QF pulse output.

No-load and start threshold registers

Start Power Threshold Setup Register (PStart)				Address: 0x 03h Default Value : 0060H				
	Bit15	14	13	12	11	10	9	Bit8
Read:	PS15	PS 14	PS 13	PS 12	PS11	PS10	PS 9	PS 8
Write:								
Reset:	0	0	0	0	0	0	0	0
	Bit7	6	5	4	3	2	1	Bit0
Read:	PS7	PS 6	PS 5	PS 4	PS 3	PS 2	PS 1	PS 0
Write:								
Reset:	0	1	1	0	0	0	0	0

Start Power Threshold Setup Register (QStart)				Address: 0x 04h Default Value : 0120H				
	Bit15	14	13	12	11	10	9	Bit8
Read:	QS15	QS 14	QS 13	QS 12	QS11	QS10	QS 9	QS 8
Write:								
Reset:	0	0	0	0	0	0	0	1
	Bit7	6	5	4	3	2	1	Bit0
Read:	QS7	QS 6	QS 5	QS 4	QS 3	QS 2	QS 1	QS 0
Write:								
Reset:	0	0	1	0	0	0	0	0

The start threshold can be configured by PStart and QStart registers. They are 16-bit unsigned numbers, and when compared, they should be compared with the high 24-bit absolute value of PowerP and PowerQ (a 32-bit signed number) to judge the start status.

When |PowerP| is smaller than PStart, PF does not output any pulse.

When |PowerQ| is smaller than QStart, QF does not output any pulse.

Gain calibration register

Power Gain Register A(GPQA)			Address: 0x05h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GPQA_15	GPQA_14	GPQA_13	GPQA_12…GPQA_3	GPQA_2	GPQA_1	GPQA_0
Write:							
Reset:	0	0	0	0	0	0	0

Power Gain Register B(GPQB)			Address: 0x06h Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	GPQB_15	GPQB_14	GPQB_13	GPQB_12…GPQB_3	GPQB_2	GPQB_1	GPQB_0

Write:							
Reset:	0	0	0	0	0	0	0

Two registers are included: GPQA and GPQB (in a binary complement format), and the MSB is a symbol bit.

GPQA is used for active / reactive power calibration of the current Channel A and the voltage channel. GPQB is used for active / reactive gain calibration of the current Channel B and the voltage channel.

The calibration range is ± 100%.

Calibration formulas: P1 = P0 (1 + GPQS)
Q1 = Q0 (1 + GPQS)

Where, GPQS is the normalized value the gain calibration register, with the use referring to Chapter III Calibration Methods.

Phase calibration register

Phase Calibration Register A(PhsA)				Address: 0x 07H		Default Value : 00H		
	Bit7	6	5	4	3	2	1	Bit0
Read:	PhsA_7	PhsA_6	PhsA _5	PhsA _4	PhsA _3	PhsA _2	PhsA _1	PhsA _0
Write:								
Reset:	0	0	0	0	0	0	0	0

Phase Calibration Register B(PhsB)			Address: 0x08 H		Default Value : 00H			
	Bit7	6	5	4	3	2	1	Bit0
Read:	PhsB _7	PhsB _6	PhsB _5	PhsB _4	PhsB _3	PhsB _2	PhsB _1	PhsB _0
Write:								
Reset:	0	0	0	0	0	0	0	0

IA and U-channel phase calibration PhsA and IB and U-channel phase calibration PhsB are included. Such two registers are both signed binary complement codes, with Bit0 ~bit7 valid, in which bit7 is the sign bit. Refer to Chapter III Calibration Method for detailed use.

1 LSB represents the delay of 1/895 kHz = 1.12us/LSB, and under 50HZ, 1 LSB represents 1.12 us * 360 ° * 50 / 10 ^ 6 = 0.02°, /LSB phase calibration.

Phase calibration range: at 50HZ, ± 2.56 °

Reactive power phase calibration register

Reactive Power Phase Calibration Register (QPhsCal)				Address: 09H		Default Value : 0000H		
	Bit15	14	13	12..3		2	1	Bit0
Read:	QPC15	QPC14	QPC13	QPC12.. QPC3		QPC2	QPC1	QPC0
Write:								
Reset:	0	0	0	0	0	0	0	0

Reactive power phase calibration register is used for phase calibration of U-channel 90° phase-shift filter in the reactive calculation. Reactive power phase calibration register adopts a 16-bit binary complement

form, and the MSB is a sign bit. Refer to Chapter III Calibration Method for detailed use.

Calibration formula: Q2 = Q1-QPhs * P1

Where, P1 is active power, Q1 is reactive power before calibration, and Q2 is reactive power after calibration.

Active Power Offset Calibration Registers

Active Power Offset Register A(APOSA)			Address: 0AH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSA_15	APOSA_14	APOSA_13	APOSA_12…APOSA_3	APOSA_2	APOSA_1	APOSA_0
Reset:	0	0	0	0	0	0	0

Active Power Offset Register B(APOSB)			Address: 0BH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	APOSB_15	APOSB_14	APOSB_13	APOSB_12…APOSB_3	APOSB_2	APOSB_1	APOSB_0
Reset:	0	0	0	0	0	0	0

Active power offset calibration registers apply to accurate calibration of small signals. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III Calibration Method for detailed use.

The APOSA register is the Offset value of the current channel-A and U active power.

The APOSB register is the Offset value of the current channel-B and U active power.

Reactive Power Offset Calibration Register

Rective Power Offset Register (RPOSA)			Address: 0CH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	RPOSA_15	RPOSA_14	RPOSA_13	RPOSA_12…RPOSA_3	RPOSA_2	RPOSA_1	RPOSA_0
Reset:	0	0	0	0	0	0	0

Rective Power Offset Register (RPOSB)			Address: 0DH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: / Write:	RPOSB_15	RPOSB_14	RPOSB_13	RPOSB_12…RPOSB_3	RPOSB_2	RPOSB_1	RPOSB_0
Reset:	0	0	0	0	0	0	0

Reactive power offset calibration register applies to accurate calibration of reactive small signals. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III

Calibration Method for detailed use.

The RPOSA register is the Offset value of the current channel-A and U reactive power. The PPOSB register is the Offset value of the current channel-B and U reactive power.

RMS Offset Calibration Registers

IA RMS Offset Register(IARMSOS)			Address: 0EH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	IARMS_15	IARMS _14	IARMS _13	IARMS _12…IARMS _3	IARMS _2	IARMS _1	IARMS _0
Reset:	0	0	0	0	0	0	0

IB RMS Offset Register(IBRMSOS)			Address: 0FH Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	IBRMS_15	IBRMS _14	IBRMS _13	IBRMS _12…IBRMS _3	IBRMS _2	IBRMS _1	IBRMS _0
Reset:	0	0	0	0	0	0	0

RMS Offset calibration registers apply to accurate calibration of small signal of current RMS. Such two registers both adopt a binary complement format with the MSB of a symbol bit. Refer to Chapter III Calibration Method for detailed use.

The IARMSOS register is the RMS Offset value of Current A. The IBRMSOS register is the RMS Offset value of Current B.

Current B Gain Settings

Current B Gain Register (IBGain)			Address: 10H Default Value : 0000H				
	Bit15	14	13	12 … 3	2	1	Bit0
Read: Write:	IBG15	IBG14	IBG13	IBG12…IBG3	IBG2	IBG1	IBG0
Reset:	0	0	0	0	0	0	0

Current B gain setting registers are used for consistency calibration of the two current channels in the anti-tampering meter. The consistency calibration is to be completed at 100% Ib point. Refer to Chapter III Calibration Method for detailed use.

Channel B current gain registers all adopt a binary complement format with the MSB of a symbol bit within (-1, +1).

If IBGain> = 2 ^ 15, then GainI2 = (IBGain-2 ^ 16) / 2 ^ 15

Otherwise, GainI2 = IBGain / 2 ^ 15

I2a (before calibration) and I2b (after adjustment) will have the following relationship: I2b = I2a + I2a * GainI2

2.12.3 Measurement parameter registers

Fast pulse counter

Active Energy Counter Register (PFCNT)				Address: 0x20h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	PFC15	PFC14	PFC13	PFC12…PFC3	PFC2	PFC1	PFC0
Write:							
Reset:	0	0	0	0	0	0	0

Reactive Energy Counter Register (QFCNT)				Address：0x21h			
	Bit15	14	13	12 … 3	2	1	Bit0
Read:	QFC15	QFC14	QFC13	QFC12…QFC3	QFC2	QFC1	QFC0
Write:							
Reset:	0	0	0	0	0	0	0

In order to prevent energy loss when power on and off, the MCU will read and save the register PFCnt / QFCnt values in case of power-fall, and then the MCU will re-write such values into PFCnt / QFCnt when later power-on.

When the fast pulse counter register PFCnt / QFCnt has 2 times of its count absolute value greater than or equal to HFconst, the corresponding PF / QF will overflow pulse, and the energy register will have its value plus 1 accordingly.

Current and Voltage RMS Registers

Current A Rms Register (IARms)				Address： 0x22h			
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IAS23	IAS22	IAS21	IAS20…IAS3	IAS2	IAS1	IAS0

Current B Rms Register (IBRms)				Address： 0x23h			
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	IBS23	IBS22	IBS21	IBS20…IBS3	IBS2	IBS1	IBS0

Voltage Rms Register (Urms)				Address： 0x24h			
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	US23	US22	US21	US20…US3	US2	US1	US0

Rms is a 24-bit signed number, the MSB = 0 indicates valid data, and the MSB = 1 indicates that the reading is treated as zero; the parameter refresh frequency will be 3.4Hz.

Voltage Frequency Register

Voltage Frequency Register (UFreq)				Address： 0x25h			
	Bit15	14	13	12 … 3	2	1	Bit0

Read:	Ufreq15	Ufreq14	Ufreq13	Ufreq12…Ufreq3	Ufreq2	Ufreq1	Ufreq0

It will mainly measure the fundamental frequency, with the measurement bandwidth of 250Hz or so.

The frequency value is a 16-bit unsigned number, with the parameter formatting formula as follows:

f=CLKIN/8/UFREQ

For example, if the system clock CLKIN = 3.579545MHz, UFREQ = 8948, then the actual frequency measured should be:

f=3579545/8/8948=49.9908Hz。

The voltage frequency measurement has its refresh cycle of 0.7s.

Average active power register

Active Power Register (PowerPA)			Address： 0x26h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APA23	APA22	APA21	APA20…APA3	APA2	APA1	APA0

Active Power Register (PowerPB)			Address： 0x27h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	APB23	APB22	APB21	APB20…APB3	APB2	APB1	APB0

The active parameter PowerP is 32-bit data in a binary complement format, with the MSB of a symbol bit. The power parameter has its refresh frequency of 3.4Hz.

POWERPA is the average active power register of Channel U and Channel IA, while POWERPB is the average active power register of Channel U and Channel IB.

Average reactive power register

Reactive Power Register (PowerQ)			Address： 0x28h				
	Bit31	30	29	28 … 3	2	1	Bit0
Read:	RP23	RP22	RP21	RP20…RP3	RP2	RP1	RP0

The reactive parameter PowerQ is 32-bit data in a binary complement format, with the MSB of asymbol bit. Its refresh frequency is same as PowerPA and PowerPB.

This register results from reactive power calculation of Channel U and user-selected current channel, and Channel A shall be selected by default.

Active energy register

Active Energy Register (EnergyP)			Address： 0x29h				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

EnergyP register is an accumulative active energy register. When 0xFFFFFF overflows to 0x000000, the overflow sign POIF (see IF 0x41H) will appear.

The energy parameter is an unsigned number, and the EnergyP register values represent the cumulative number of PF pulses respectively. The register has its smallest unit representing the energy of 1/EC kWh, in which EC is the meter constant.

Active Energy Register 2

Active Energy Register2 (EnergyP2)			Address： 0x2AH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

EnergyP2 register is a active energy register which is cleared after read.

Reactive Energy Register

REActive Energy Register (EnergyQ)			Address： 0x2BH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23	EP22	EP21	EP20…EP3	EP2	EP1	EP0

EnergyQ register is an accumulative reactive energy register. When 0xFFFFFF overflows to 0x000000, the overflow sign QOIF (see IF 0x41H) will appear.

The reactive energy parameter is an unsigned number, and the EnergyQ register values represent the cumulative number of QF pulses respectively. The register has its smallest unit representing the energy of 1/EC kVARh, in which EC is the meter constant.

Reactive Energy Register 2

REActive Energy Register2 (EnergyQ2)			Address： 0x2CH				
	Bit23	22	21	20 … 3	2	1	Bit0
Read:	EP23_2	EP22_2	EP21_2	EP20_2…EP3_2	EP2_2	EP1_2	EP0_2

EnergyQ2 register is a reactive energy register which is cleared after read.

EMU Status Registers

The EMU status registers include measurement status registers and checksum registers.

EMU STATUS Register (EMUStatus) Address：0x2D h read-only register		
Bit	**Bit Name**	**Descriptions of Functions**
23-22	Reserved	Reserved
21	CHNSEL	Status sign bit for current channel selection: = 1 indicates that the current channel currently used to calculate the active / reactive power is Channel B; = 0 indicates that the current channel currently used to calculate the active / reactive power is Channel A. This bit is 0 by default, and refers to Channel A is used to measure the energy.
20	Noqld	When reactive power is less than the starting power, NoQld is set as 1; when reactive power is greater than / equal to the starting power, NoQld is reset.

19	Nopld	When active power is less than the starting power, NoPld is set as 1; when active power is greater than / equal to the starting power, NoPLd is reset.
18	REVQ	Indication and identification signal of inverse reactive power - When negative reactive power is detected, this signal is 1. When positive reactive power is detected again, this signal is 0. This value will be updated when QF is producing pulse.
17	REVP	Indication and identification signal of inverse active power - When negative active power is detected, this signal is 1. When positive reactive power is detected again, this signal is 0. This value will be updated when PF is producing pulse.
16	ChksumBusy	Calibration data checksum calculation status register ChksumBusy = 0 indicates that the calibration data checksum calculation has been completed. The checksum value is available. ChksumBusy = 1 indicates that the calibration data checksum calculation has not been completed. The checksum value is not available.
15:0	Chksum	Checksum output

EMUStatus [15:0] is a register specifically provided by RN8209G to store the 16-bit checksum of calibration parameter configuration registers, and the external MCU can detect this register to monitor whether the calibration data is confused.

The checksum is calculated with double-byte accumulation then inversed. For the single-byte register PHSA / PHSB, it should be accumulated after extended to be a double byte, and the extended byte should be 00H.

The register address for RN8209G to conduct checksum calculation is 00H-10H, and the checksum calculated on the basis of RN8209G default value is 0xEE79.

Given the following three cases, re-start a checksum calculation: the system is reset, some 00H-10H register has WRITE operations, and EMUStatus register has READ operations. One time of checksum calculation needs 11.2us.

2.12.4 Interrupt Register

Interrupt configuration and enable register

This register applies to SPI and RSIO. When the interrupt enable bit is configured as 1 and the interrupt occurs, the IRQ_N pin will output a low level. Write-protect register – Before configuration of this register, the write enable needs to be opened.

Interrupt Enable Register (IE) Address: 0x40H default: 0x00H readable and writable		
Bit	**Bit Name**	**Descriptions of Functions**
7-6	Reserved	Reserved, read as 0
5	ZXIE	ZXIE = 0: Disable the zero-crossing interrupt; ZXIE = 1: Enable the zero-crossing interrupt.
4	QEOIE	QEOIE = 0: Disable reactive energy register overflow interrupt; QEOIE = 1: Enable reactive energy register overflow interrupt.
3	PEOIE	PEOIE = 0: Disable active energy register overflow interrupt; PEOIE = 1: Enable active energy register overflow interrupt.
2	QFIE	QFIE = 0: Disable the QF interrupt; QFIE = 1: Enable the QF interrupt.
1	PFIE	PFIE = 0: Disable the PF interrupt; PFIE = 1: Enable the PF interrupt.

0	DUPDIE	DUPDIE = 0: Disable the data update interrupt; DUPDIE = 1: Enable the data update interrupt. The data PowerPA / PowerPB, PowerQ, IARMS / IBRMS and URMS registers have the refresh frequency of 3.4HZ, and when the above-mentioned data is updated, the IRQ_N pin will output a low level.

Interrupt status register

Interrupt Flag Register (IF) Address: 0x41H read-only		
Bit	**Bit Name**	**Descriptions of Functions**
7-6	Reserved	Reserved
5	ZXIF	ZXIF = 0: No zero-crossing event occurs; ZXIF = 1: zero-crossing event occurs.
4	QEOIF	QEOIF = 0: There is no reactive energy register overflow event occurring; QEOIF = 1: There is some reactive energy register overflow event occurring.
3	PEOIF	PEOIF = 0: There is no active energy register overflow event occurring; PEOIF = 1: There is some active energy register overflow event occurring.
2	QFIF	QFIF = 0: No QF pulse output event occurs; QFIF = 1: Some QF pulse output event occurs.
1	PFIF	PFIF = 0: No PF pulse output event occurs; PFIF = 1: PF pulse output event occurs.
0	DUPDIF	DUPDIF = 0: No data update event occurs; DUPDIF = 1: data update event occurs.

IF applies to SPI and RSIO interfaces. When some interrupt event occurs, the hardware will set the corresponding interrupt flag as 1.

IF interrupt flags can be generated not subject to the control of interrupt enable register IE, but to the occurrence of the interrupt event.

IF is a read-only register and will be cleared after read.

Reset Interrupt Flag Register

Reset Interrupt Flag Register (RIF)			Address： 0x42H					
	Bit7	6	5	4	3	2	1	Bit0
Read:	0	0	RZXIF	RQEOIF	RPEOIF	RQFIF	RPFIF	RDUPDIF

The bit definitions of SPI and RIF are the same as IF, and when some interrupt event occurs, the corresponding interrupt flag will be set as 1,and cleared after read, and to read RIF can clear IF and RIF registers.

RIF is designed so that SPI could still receive new interrupts while reading the interrupt flag register, with the details referring to instructions in interrupt-related sections.

For RSIO, this register is read only, read as 0, and reading RIF will not reset IF.

2.12.5 System Status Register

System Status Register

System Status Register (SysStatus) Address: 0x43H read-only		
Bit	**Bit Name**	**Descriptions of Functions**

7-5	Reserved	Reserved
4	WREN	Write enable flag: = 1 means that it allows writing in registers with write-protection; = 0 means that it allows no writing in registers with write-protection
3	Reserved	Reserved
2	IS	Pin status bit of the selection of serial communication type, used to determine the type of chip communication interfaces. IS = 0 means that RSIO is selected as the communication interface; IS = 1 means that SPI is selected as the communication interface.
1	Reserved	Reserved
0	RST	Hardware reset flag - When the external RST_N pin or power-on reset has ended, this bit is set as 1. Reset after read. It can be used as a calibration data request after reset.

SPI / RSIO read checkout register

The RData (0x44H) register holds the previous SPI / RSIO read-out data, able to be used for checkout when SPI / RSIO has read out data.

SPI / RSIO write checkout register

The WData (0x45H) register holds the previous SPI / RSIO written data, able to be used for checkout when SPI / RSIO has written data.

2.12.6 Special commands

Command Name	Command Register	Data	Description
Write enable command	0xEA	0xE5	Enable WRITE operations
Write-protect command	0xEA	0xDC	Disable WRITE operations
Current Channel A Selection Command	0xEA	0x5A	Current Channel A setting command – To specify the current channel currently used to calculate the active energy / reactive energy / reactive power as Channel A; Only when the write has been enabled, the system can accept this command; the CHNSEL register bit in the energy measurement status register reflects the implementation results of this command.
Current Channel B Selection Command	0xEA	0xA5	Current Channel B setting command – To specify the current channel currently used to calculate the active energy / reactive energy / reactive power as Channel B; Only when the write has been enabled, the system can accept this command; the CHNSEL register bit in the energy measurement status register reflects the implementation results of this command.

Scope of write protection:

0x00h-0x10h calibration parameter configuration registers, 0x20h-0x21h fast pulse registers and 0x40h interrupt enable registers, can not be modified unless special commands are adopted to enable the write, and the specific command formats are as shown in the above table.

3 Calibration Methods

3.1 Overview

RN8209G provides rich calibration means to achieve software calibration, and the calibrated meter can have the accuracy of active and reactive power up to 0.5S. RN8209G includes the following calibration means:

- Provide adjustable meter constant (HFConst)
- Provide Channel A / B gain and consistency calibration
- Provide Channel A / B phase calibration
- Provide Channel A / B active, reactive and RMS offset calibration
- Provide reactive phase calibration
- Provide small-signal speedup calibration
- Provide automatic checksum of calibration data

3.2 Calibration Flow and Parameter Calculation

While calibrating the single-phase liquid crystal meter designed for RN8209G, a standard meter shall be provided. When the standard meter is used for calibration, the active / reactive energy pulse PF / QF can be directly connected to the meter via an optical coupler, and then RN8209G can be calibrated according to the error reading of the standard meter.

3.2.1 Calibration Flow

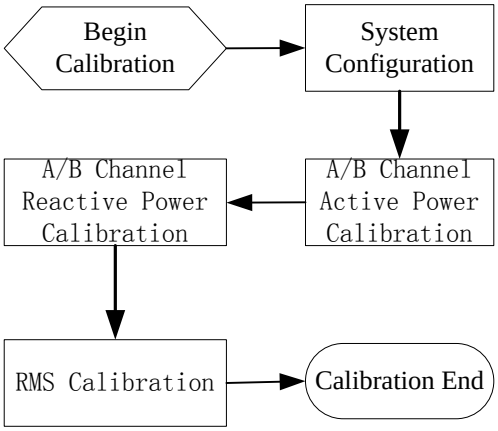


Figure 3-1 Calibration Flow

3.2.2 Parameter Settings

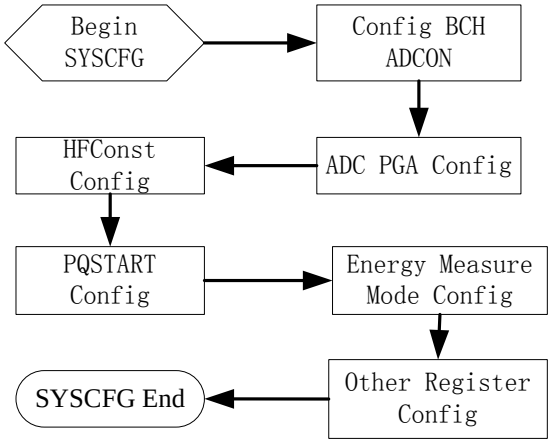


Figure 3-2 Parameter Settings Flow

HFConst parameter calculation:

When osci = 3.579545MHz, HFConst is calculated as follows:

HFConst＝INT[23.2075*Vu*Vi*10^11/(EC*Un*Ib)]

Vu: In time of rated voltage input, the voltage of voltage channel (pin voltage × magnification)

Vi: In time of rated current input, the voltage of current channel (pin voltage × magnification)

Un: Rated input voltage; Ib: Rated input current; EC: meter constant

Lookup of HFConst parameters:

In a typical application: 1) Manganin shunt adopts 400 micro-ohm; 2) IA PGA configure as 16 times; 3) Under the input conditions of 220mV sampling voltage, you can directly check up the HFConst value in the following table according to the meter constant EC and fill in the register:

EC	HFConst	EC	HFConst
800	0x4000	12800	0x0400
1600	0x2000	25600	0x0200
3200	0x1000	51200	0x0100
6400	0x0800		

3.2.3 Active Calibration

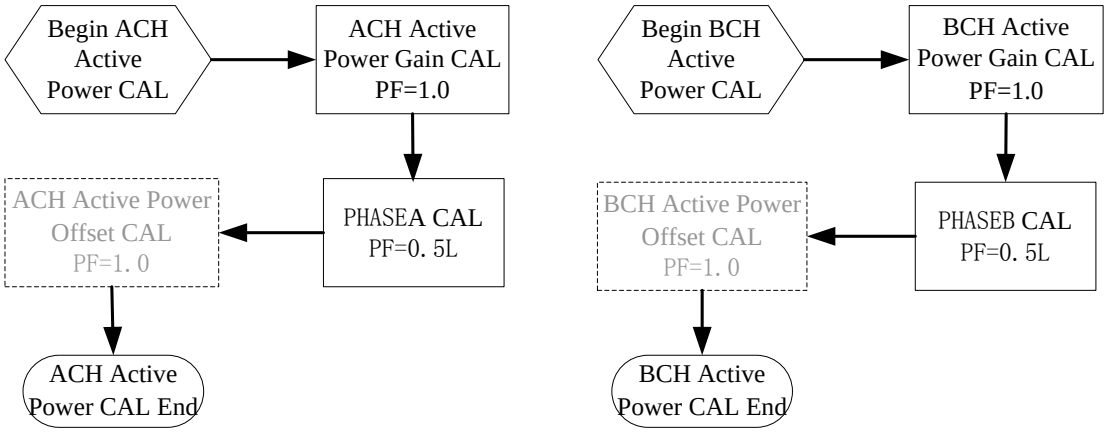


Figure 3-3 Active Calibration Flow

1. Channel A power gain calibration can be achieved by configuring a GPQA register, with GPQA calculated as follows:

Suppose the standard meter has the read error of err when Channel A is 100% Ib and PF = 1:

$$Pgain = \frac{-err}{1+err}$$

If Pgain>=0, then GPQA=INT [Pgain*2^{15}]

Otherwise, Pgain<0, then GPQA=INT [2^{16}+Pgain*2^{15}]

Channel B power gain calibration can be achieved by configuring a GPQB register, same as GPQA.

2. Calculation of Channel A / B phase calibration registers:

If the standard meter has the read error of err in Channel A / B, 100% Ib, PF = 0.5L, then the phase calibration formula is as follows:

$$\theta = \text{Arcsin}\ \frac{-err}{\sqrt{3}}$$

For 50HZ, PHSA/B features the relation of 0.02^0/LSB, then

If θ>=0, PHSA/B = INT ($\theta/0.02^0$)

If θ<0, PHSA/B =INT ($2^8+\theta/0.02^0$)

3. Active offset calibration is an effective means to improve the small-signal active accuracy if the external noise (PCB noise, transformer noise, etc.) is greater and the integrated energy has impact on the accuracy of small signals. If the external noise has comparatively small impact on the small-signal active accuracy, this step can be ignored.

3.2.4 Reactive Calibration

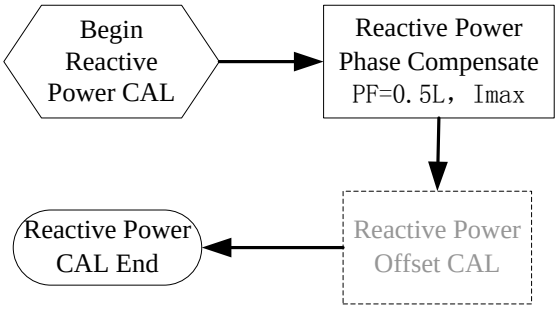


Figure 3-4 Reactive Calibration Flow

1 Reactive phase calibration registers are used as phase calibration of U-channel 90° phase-shift filter in the reactive calculation under large-signal conditions. Reactive phase calibration registers are calculated as follows:

If the standard meter has the read-out error of err in Channel A, Imax and PF = 0.5L (60 º), then:

α= -error / cot (θ) = -error * 0.5774

If α>=0, then Qphs=INT [$\alpha*2^{15}$]; if α< 0, then Qphs=INT [$2^{16}+\alpha*2^15$]

If α> = 0, then Qphs = INT [α * 215]; if α <0, then Qphs = INT [216 + α * 215]

Note: Qphs calculation needs Channel A active power, so the calibration of this step must be completed after active calibration.

2. Reactive offset calibration is an effective means to improve the small-signal reactive accuracy if the external noise (PCB noise, transformer noise, etc.) is greater and the integrated energy has impact on the accuracy of small signals. If the external noise has comparatively small impact on the small-signal active accuracy, this step can be ignored.

3.2.5 RMS Calibration

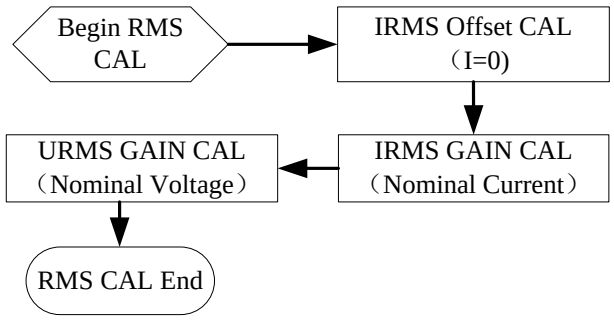


Figure 3-5 RMS Calibration Flow

Descriptions:

1. Current offset calibration can improve the small-signal current RMS accuracy.

The process for IARMSOS register calculation is as follows:

1) A standard meter support shall be configured so that U = Un and the current input is Vi = 0;
2) Wait for updates of DUPDIF identification bit (about 3.4Hz refresh per second);
3) MCU takes the IARMS register value for temporary storage;
4) Repeat Step 2 and Step 3 for eleven times, with the first data able to be ignored. The MCU takes the following data to obtain the average of Iave;
5) Find the Iave ^ 2;
6) Find its 32-bit binary complement code, take the sign bit to fill in bit15 of the IARMSOS register, and take bit23 ~ bit8 to fill in IRMSOS bit14 ~ bit0 to obtain IRMSOS;
7) The rms offset calibration is completed.

So do the IBRMS calibration formula and the process of IBRMSOS register calculation.

2. When the current offset is well calibrated, then calibrate the current conversion factor KiA / KiB and the voltage conversion factor Ku of Channel A / B, which shall be completed by the MCU, with the calculation process as follows:

If the IARMS register has its reading as RMSIAreg in case of the rated current Ib, then

KiA＝Ib/RMSIAreg

Where, KiA is the ratio of the rated value and corresponding register in case of rated input.

Channel B conversion factor KiB can be calculated the same as the voltage conversion factor Ku.

3.3 Examples

Assuming a sample meter features a 220v (Un), 5A (Ib) rated input, with the meter constant of 3200 (EC). Channel A current sampling adopts 350 micro-ohm Manganin shunt, and Channel A has its analog gain of 16 times; Channel B current sampling adopts current transformers, and Channel B has its analog gain selected as 1 time (1X); the voltage channel adopts resistor divider input, the analog channel gain features 1 time and the chip pin voltage value is 0.22v.

1 Calculate HFConst

Vu＝0.22V; Vi＝5*0.00035*16＝0.028V; EC=3200; Un=220; Ib=5.

HFConst=[23.2075*Vu*Vi*10^11/(EC*Un*Ib)]=4061.1

After rounded, HFConst will be FDDH (4061). And just write this value in HFCONST register.

2. Channel A Active Calibration

1) Channel A gain calibration

If the power source outputs a 220v and 5A signal with the power factor of 1, and the error displayed on the standard meter is 1.2%, then

Pgain＝-0.012/(1+0.012)=--0.01186

If this number is less than 0 and needs to be converted into a complement code, then

0.01186*2^15+2^16=0xFE7BH

Write FE7Bh into the GPQA register to complete gain calibration of Channel A.

2) Channel A phase calibration

After the resistive gain has been calibrated, the power factor will be changed to 0.5L, and if the error displayed on the standard meter is -0.4%, then

θ=ArcSin（-(-0.004)/1.732）=ArcSin 0.0023 ＝ 0.1323^0

phs=INT[0.1323/0.02]=6

After rounded, it will be 0x06H, and just write it into the angle calibration register PHSA.

3) Channel A active OFFSET calibration

If the current input is zero, the active power register has its value read as 0Xfffff50f (several times of average can be read), and its 32-bit complement code is 0x00000AF1. Take the latter 4 digits (0X0AF1) and write into the active offset calibration register.

Channel B active calibration is similar to Channel A.

3. Reactive Power Calibration

1) Reactive phase calibration

After the active calibration is completed, the reactive power only needs to accept phase calibration. At the reactive power point 0.5L (60º), the error displayed on the standard meter is -0.04%, then

α= -0.0004*0.577= -0.0002308<0, Qphs=INT (2^16-.0002308*2^15) = 65528=0xfff8

Write the hexadecimal FFF8 into the reactive phase calibration register.

2) Reactive Offset

If the current input is zero, the reactive power register has its value read as 0XFFFFF47D (several times of average can be read), and its 32-bit complement code is 0x00000B83. Take the latter 4 digits (0X0B83) and write into the reactive offset calibration register.

4 RMS Calibration

The chip provides the current RMS offset calibration register, and if the current input is zero, the current rms register has its value read as 0x000483 (several times of average can be read), with the decimal number of 1155.

Square it to find its complement code: 1155*1155=1334025=0x145B09, 32-bit complement code to be 0Xffeba4f7.

Take the middle four digits 0xeba4 and write in the current rms offset calibration register.

The conversion factor shall be calculated by the MCU.

4 Communication Interfaces

- Two kinds of serial communication interfaces are supported: SPI and RSIO, which are working in a slave mode;
- The serial communication interface options shall be set via the external pin IS;
- SPI and RSIO interfaces are compatible with 5V/3.3V;

4.1 SPI Interface

4.1.1 Descriptions of SPI Interface Signals

SCSN: SPI slave device chip select signal, active at low levels, input signal, internal floating, and external pull-up resistors recommended.

When SCSN is changing from high to low, it indicates that the current chip is selected and in the communication state; when SCSN from low to high, it means that the communication has ended, and the communication port is reset to an idle state.

SCLK: serial clock input pin – it decides the transmission rate of data in or out of the SPI port.

All data transmission operations are synchronized with SCLK, RN8209G outputs data from the SDO pin at the rising edge; the host outputs data from the SDI pin at the rising edge. RN8209G and the host will read data at the falling edge.

SDI: Serial data input pin – Used to transmit the master data to RN8209G inside.

SDO: serial data output pin- Used to output the RN8209G data to the master. It stays in high impedance when SCSN is in a high level.

4.1.2 SPI Frame Format

SPI frames include reading frames, writing frames and special command frames. Each frame has its transmission process as follows:

When RN8209G detects SCSN falling edge, SPI will enter the means of communication, and in this mode, RN8209G will wait for the MCU to transmit the command bytes to the command register.

The command register is a 8-bit wide register. For the read and write operations, bit7 of the command register will be used to determine whether this data transmission operation is a read or write operation, and bit6-0 of the command register is a read-write register address. For the special command operations, the command register has its bit7-0 fixed to be 0xEAH.

After the command register has been written, chip analysis and response the command, the data transmission will start. After data transmission is completed, SPI will enter a communication mode again, waiting for the CPU to transmit new command bytes to the command register.

These three types of SPI frame formats are described in Table 4-1.

Table 4-1 SPI Frame Formats

Command Name	Command Register	Data	Descriptions
Read command	{0,REG_ADR[6:0]}	RDATA	Read data from a register with the address of REG_ADR [6:0]. Note: If an invalid address is read, the return value is 00h.
Write command	{1,REG_ADR[6:0]}	WDATA	Write data to the register with the address of REG_ADR [6:0].
Write Enable Command	0xEA	0xE5	See Section 2.12.6 Special Commands
Write-Protect Command	0xEA	0xDC	
Command for Current Channel A Selection	0xEA	0x5A	
Command for Current	0xEA	0xA5	

Channel B Selection			

4.1.3 SPI Write Operation

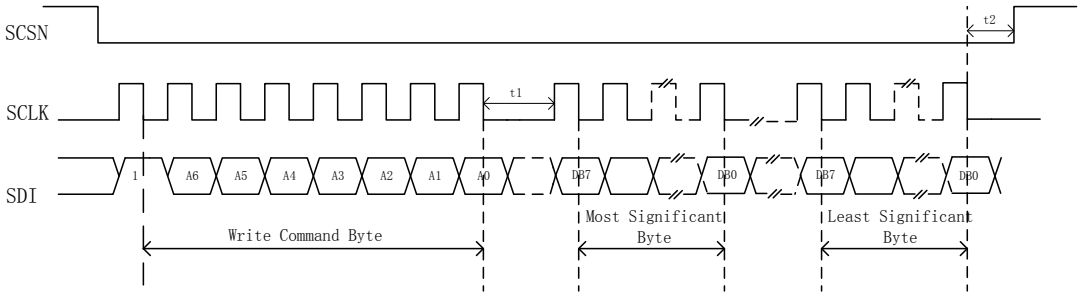


Figure 4-1 SPI Write Timing

Work process:

If the SCSN is valid, then the host will write in command bytes (8bit, including the register addresses) via SPI, and then write in data bytes. Note:

1. Transmit in bytes, high bit first while low bit later;
2. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;
3. The host writes in data at the SCLK rising edge while the slave reads data at the SCLK falling edge;
4. The time t1 between data bytes should be greater than or equal to half SCLK cycle;
5. After the LSB of the last byte has been transmitted, the SCSN will change from low to high and end data transmission. The time t2 between the SCLK falling edge and the SCSN rising edge should be greater than or equal to half SCLK cycle.

Note: The registers with write protection should have write enable command written in at first before write operations.

4.1.4 SPI Read Operation

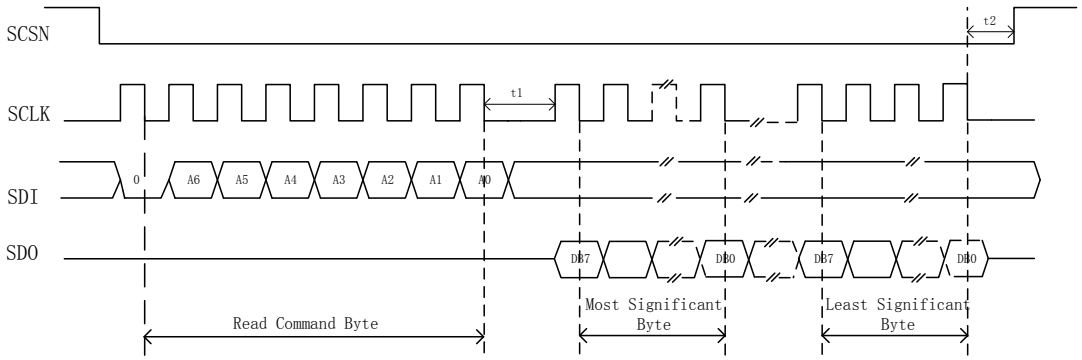


Figure 4-2 SPI Read Timing

Work process:

If the SCSN is valid, then the host will write in command bytes (8bit, including the register addresses) via SPI, and the slave will output the data in bytes from the SDO pin at the SCLK rising edge. Note:

1. Transmit in bytes, high bits first while low bits later;
2. Multi-byte registers will first transmit high-byte contents followed by low-byte contents;
3. The host writes in command bytes at the SCLK rising edge while the slave outputs data from SDO at the SCLK rising edge;
4. The time t1 of data bytes should be greater than or equal to half SCLK cycle;

5. After the LSB of the last byte has been transmitted, the SCSN will change from low to high and end data transmission. The time t2 between the SCLK falling edge and the SCSN rising edge should be greater than or equal to half SCLK cycle.

4.1.5 SPI Interface Reliability Design

The SPI interface reliability design includes the following contents:

- Checkout functions
  1. Provide the checkout register EMUStatus (0x2DH) to store the checksum of internal calibration registers.
  2. Provide the SPI read checkout register RData (0x44H) to save the previous SPI read-out data.
  3. Provide the SPI write checkout register WData (0x45H) to save the previous SPI written-in data.
- Write protection

  Provide write-protect features for all readable and writable registers.
- Application circuit design

The SPI transmission signal lines may vibrate subject to interference so the external resistors and capacitors are necessary for filtering. The parameters can be selected according to needs.

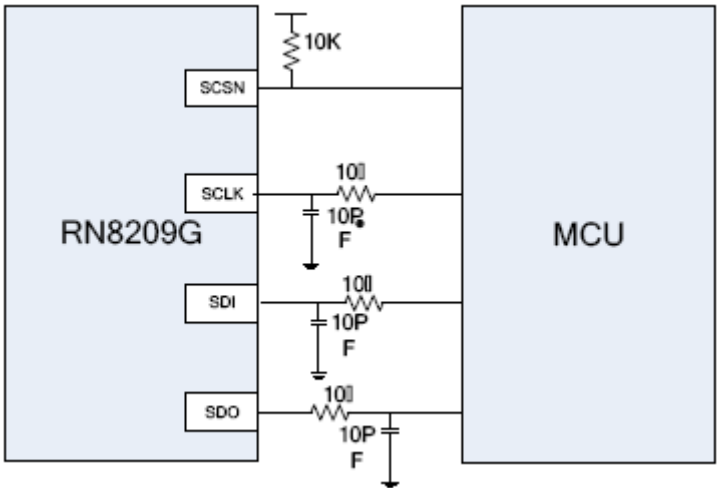


Figure 4-3 SPI Typical Connection

4.2 RSIO Interface

RN8209G supports RENERGY proprietary RSIO bus. The RSIO bus can achieve two-way communications between the CPU and the measurement chip only by means of one line.

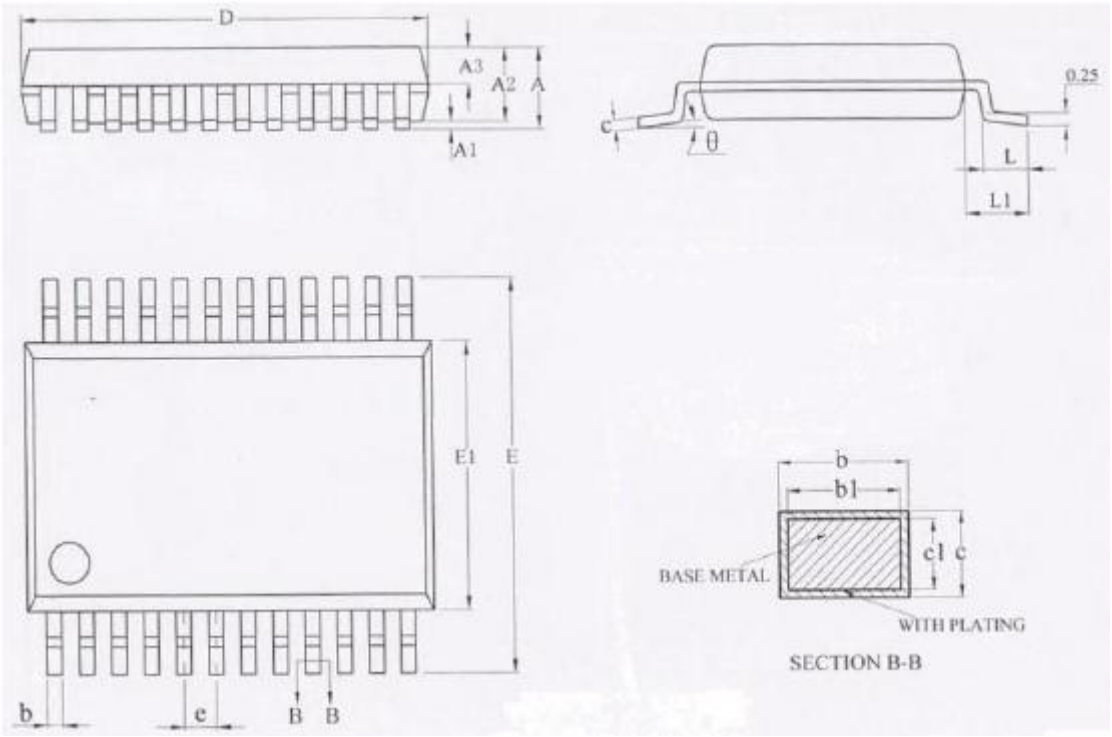
See documentation of <RENERGY Single-wire Communication Protocol>.

5 Electrical Specification

Accuracy (V_{dd}=AV_{dd}=5V±5%, room temperature)						
Measured Items	**Symbol**	Min.	Typical	Max.	Unit	Test Conditions and Notes
Active energy measurement error	Err			±0.1%		At room temperature 1500:1 dynamic range
Active energy measurement bandwidth	BW		14		kHz	OSCI=3.579545MHz
Reactive energy measurement error	Err			±0.1%		At room temperature 1500:1 dynamic range
RMS measurement error	Err			±0.5%		At room temperature 400:1 dynamic range
Analog Input						
Maximum signal level	V_{xn}			±700	mV	
DC input impedance	Z_{DC}	300			kΩ	
ADC offset error	DC_{off}		10		mV	
-3dB bandwidth	B_{-3dB}		14		kHz	OSCI=3.579545MHz
Reference Voltage (V_{dd}=AV_{dd}=5V±5%, temperature range: -40 ℃ ~ +85 ℃)						
Output voltage	Vref	2.45	2.5	2.55	V	Standard deviation < 0.01V
Temperature coefficient	Tc		25		ppm/℃	
Input impedance			4		kΩ	
Clock Input						
Range of input clock frequency	OSCI	1	3.58	4	MHz	
Interface speed						
SPI interface speed		1K		1.2M	Hz	
Single-wire interface speed		500		10K	Hz	
Power Supply						
Analog power	AVDD	4.5		5.5	V	5V±10%
Digital power	DVDD	4.5		5.5	V	5V±10%
Analog Current 1	AIdd1		2.7		mA	Channel B ADC closed
Analog Current 2	AIdd2		3.6		mA	Channel B ADC open
Digital current	DIdd		2.9		mA	OSCI=3.579545MHz
Absolute Maxium Ratings						
Digital supply voltage	DVDD	-0.3	--	＋7	V	
Analog supply voltage	AVDD	-0.3	--	＋7	V	
DVDD to DGND		-0.3	--	＋7	V	

DVDD to AVDD		-0.3		+0.3	V	
V1P,V1N,V2P,V2N		-6		+6	V	
Digital input voltage relative to GND	V_{IND}	-0.3	--	DV_{DD} +0.3	V	
Digital output voltage relative to GND	V_{outD}	-0.3	--	DV_{DD} +0.3	V	
Analog input voltage to AGND	V_{INA}	-0.3	--	AV_{DD} +0.3	V	
Range of operating temperature	T_A	-40	--	85	℃	
Range of storage temperature	T_{stg}	-65	--	150	℃	

6. Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.85
A1	0.05	0.15	0.25
A2	1.30	1.50	1.70
A3	0.57	0.67	0.77
b	0.29	---	0.37
b1	0.28	0.30	0.33
c	0.15	---	0.20
c1	0.14	0.15	0.16
D	8.00	8.20	8.40
E	7.60	7.80	8.00
E1	5.10	5.30	5.50
e	0.65BSC		
L	0.75	0.90	1.05
L1	1.25BSC		
θ	0	-----	8º